CLAIMS

What is claimed is:

1. A method (300) for detecting resistive bridge defects (105) in a global data bus (155) of a semiconductor memory having N Z-blocks (150) comprising: a) providing a plurality of data sets according to a predetermined test pattern (310) suitable for detecting the resistive bridge defects; b) using the plurality of data sets, performing write and read operations (320) to at least a predetermined memory position within a Z-block of the N Z-blocks of the semiconductor memory such that each data set is applied to each of the at least a predetermined memory position; and, c) repeating (330) the steps a ) and b) for a plurality of the N Z-blocks of the semiconductor memory.

2. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 1 wherein the plurality of Z-blocks comprises the N Z-blocks of the semiconductor memory.

3. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 2 wherein the at least a predetermined memory position includes fewer than all memory positions of the Z-block.

4. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 3 wherein the at least a predetermined memory position comprises the highest memory position.

5. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 3 wherein the at least a predetermined memory position comprises all bit columns of the Z-block and a predetermined portion of rows of the Z-block.

6. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 5 wherein the memory positions are determined in a diagonal fashion (200).

7. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 5 comprising repeating the steps a) and b) for a same Z-block.

8. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 7 wherein the steps a) and b) are repeated at least four times.

9. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks comprising: a) providing a plurality of data sets according to a predetermined test pattern for detecting the resistive bridge defects; b) using the plurality of data sets, performing write and read operations to at least a predetermined memory position within a Z-block of the N Z-blocks of the semiconductor memory such that each data set is applied to each of the at least a predetermined memory position; c) repeating the steps a) and b); and, d) repeating the steps a ) to c) for a plurality of the N Z-blocks of the semiconductor memory.

10. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 9 wherein the at least a predetermined memory position is less than all memory positions of the Z-block.

11. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 10 wherein the plurality of Z-blocks comprises the N Z-blocks of the semiconductor memory.

12. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 11 wherein the at least a predetermined memory position comprises all bit columns of the Z-block and a predetermined portion of rows of the Z-block.

13. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 12 wherein the memory positions are determined in a diagonal fashion.

14. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 13 wherein the steps a) and b) are repeated at least four times.

15. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 14 wherein the at least a predetermined memory position comprises the highest memory position.

16. A method for detecting resistive bridge defects in a global data bus of a read-only semiconductor memory having N Z-blocks comprising: a) determining a plurality of data sets according to a predetermined test pattern for detecting the resistive bridge defects; b) reading data corresponding to the determined plurality of data sets out of at least a predetermined memory position within a Z-block of the N Z-blocks of the semiconductor

memory; and, c) repeating the steps a ) and b) for a plurality of the N Z-blocks of the semiconductor memory.

17. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 16 wherein the plurality of Z-blocks comprises the N Z-blocks of the semiconductor memory.

18. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 17 wherein the at least a predetermined memory position comprises the highest memory position.

19. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 17 wherein the at least a predetermined memory position is less than all memory positions of the Z-block.

20. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 17 comprising repeating the steps a) and b) for a same Z-block.

21. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 20 wherein the steps a) and b) are repeated at least four times.

22. A method for detecting resistive bridge defects in a global data bus of a semiconductor memory having N Z-blocks as defined in claim 17 wherein data corresponding to a determined data set comprises a plurality of data subsets consecutively read out of different memory positions.